REMARKS

Remaining Claims

Claims 1, 2, and 4 – 24 remain pending in this application. Claims 1, 19 – 21, and 23 have been amended herein. The Applicant respectfully requests reconsideration and that the amendment being submitted herewith be entered.

Allowed Claims

Claims 11 – 18 have been allowed by the Examiner. The Applicant wishes to thank the Examiner for recognizing the allowability of these claims.

Objected to Claims

Claim 2 stands objected to as being dependent upon a rejected base claim. The examiner has indicated that this claim would be allowable if rewritten in independent form to include all of the limitations of claim 1. The Applicant wishes to thank the Examiner for recognizing the allowable subject matter of this claim. The Applicant believes that claim 1 as amended by the amendment being filed herewith is allowable over the prior art of record, and therefore has chosen not to rewrite claim 2 in independent form to include the limitations of claim 1.

Rejection of Claim 5 under 35 USC §112, second paragraph

Claim 5 stands rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Specifically, the Examiner points out that the element "said first one of said first flip flops" in claim 5 lacks antecedent basis. The Applicant apologizes for the oversight. This element in claim 5 has been changed to "said first one of said flip flops". In view of this amendment to claim 5, the Applicant respectfully submits that this rejection is overcome and requests that it be withdrawn.

Rejection of Claims 1, 4, 6-10 and 19-24 under 35 USC §102(b) – Gujral et al.

Claims 1, 4, 6-10 and 19-24 stand rejected under 35 USC §102(b) as being anticipated by Gujral et al. (U.S. Patent No. 5,896,052). This rejection is believed to be moot in view of the amendments to the independent claims. Nevertheless, the merits of the rejection will be addressed.

The pulse synchronizer circuit disclosed in Gujral, et al. is not directed to synchronizing the transfer of data, as is the clock ration data synchronizer of the present invention. Gujral, et al. is directed to synchronizing a pulse, such as a control signal, that occurs in one clock domain to another clock domain. Col. 1, line 55 – Col. 2, line 6 of Gujral, et al. describes a synchronizer for synchronizing "a signal which represents some event, such as loading a register, clearing a counter, or detecting an error ... commonly represented by a short pulse." This portion of Gujral, et al. also states: "[w]e have developed 'pulse synchronizers' designed to handle just such situations. Two such synchronizers are described here; each has different characteristics and restrictions on the types of pulses it will synchronize." The text goes on to state: "[I]t is an object hereof to address such needs, and provide related features. A related object is to teach 'pulse synchronizer' means, e.g., to address metastability where a logic circuit involves multiple asynchronous clocks."

It is clear from the above-quoted language that Gujral, et al. is not directed to synchronizing the transfer of data between clock domains, but is directed to synchronizing control signals and the like between clock domains. In contrast, the present invention is directed to synchronizing the transfer of data between clock domains, as recited in the independent claims of the present application. In fact, Gujral, et al. is incapable of being used for synchronizing the transfer of data between clock domains. Gujral, et al. discloses two embodiments, the first of which is shown in Fig. 2 and the second of which is shown in Fig. 3. With respect to the embodiment shown in Fig. 2, Col. 3, lines 10 – 15, states: "[o]ne restriction on the use of this circuit is that the input signal must present pulses that are a single clock period in width". With respect to the embodiment shown in Fig. 3, Col. 3, lines 48 – 51, states: "[s]ince the circuit detects the rising edge of the input signal, the signal can transition high and remain high indefinitely, yet the output in this case will still be a single clock pulse, one clock wide."

It is clear from the description of these two embodiments that the pulse synchronizers disclosed in Gujral, et al. cannot be used to transfer data. With respect to the embodiment shown in Fig. 2, because restrictions are placed on the width of the input data, the circuit cannot be used to transfer data from one clock domain to another. If the data has a width that is greater than the width of one clock pulse, the circuit will not work. For example, if data being transferred is a series of 1's, the data is represented by a signal that remains high for a number of clock cycles. The circuit shown in Fig. 2 of Gujral, et al. will not work in this case because the signal remains high for longer than one clock pulse.

With respect to the embodiment shown in Fig. 3, the output signal will always be a single clock pulse in width. Therefore, the circuit cannot be used to transfer data because if the data is more than one clock pulse in width, the data will be truncated to one clock pulse. For example, if a series of 1's are being transferred over a series of clock cycles, the output section of the circuit shown in Fig. 3 will truncate the series of 1's to a pulse that is high for one output clock cycle and then low after that. Therefore, the circuit shown in Fig. 3 cannot be used for transferring data.

For all of these reasons, Gujral, et al. does not teach a data synchronizer or a method for synchronizing data, as recited in the independent claims of the present application. For at least these reasons, the Applicant respectfully submits that claims 1, 4, 6 – 10 and 19 – 24 are patentable over Gujral, et al., and respectfully requests that the rejection be withdrawn.

Furthermore, as stated above, in Gujral, et al. the clocks are asynchronous (See Col. 2, lines 3 – 6; Col 3, lines 7 – 9; claim 1). In contrast, the clocks of the clock ratio data synchronizer of the invention are "ratioed" in that an edge of one of the clocks is aligned with an edge of the other clock periodically. For example, the present application describes an example embodiment in which the ratio of the input clock to the output clock is 5:4. As shown in Fig. 2 of the present application, the clocks are aligned on the edges represented by reference numerals 26A and 26B. The clocks then realign on the edges represented by reference numerals 27A and 27B. Thus, in this example, the clocks align on the rising edges of every fifth pulse of the input clock and every fourth pulse of the output clock. The clock ratio data synchronizer of the present invention is capable of achieving a variety of clock ratios, such as, for example, 1:2, 2:3, 3:4, 4:5, 2:1, 3:2, 4:3, etc. Synchronizing the clocks in this way allows skew tolerance margins and setup time margins to be maximized, which are among the primary goals of the invention. These features of the invention are not taught or suggested by Gujral, et al. The independent claims have been amended to clarify that the clocks are synchronized at regular intervals. For these additional reasons, the Applicant respectfully submits that the claims are patentable over Gujral, et al.

CONCLUSION

For the reasons set forth above, it is respectfully submitted that all pending claims are now in condition for allowance, and Applicant requests a Notice of Allowance be issued in this case. Should there be any further questions or concerns, the Examiner is urged to telephone the undersigned to expedite prosecution.

Respectfully submitted,
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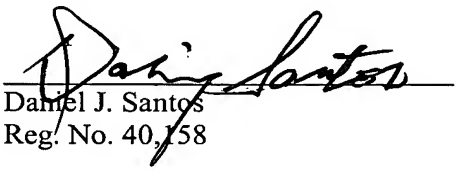

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